A 5GHz Fast-Switching CMOS Frequency Synthesizer

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Abstract — **A 5GHz PLL-based frequency synthesizer for wireless LAN applications is presented in this paper. The proposed PLL is designed using 0.25μm CMOS technology with 3.3V power supply. The enlarged VCO tuning range gives extra bandwidth to achieve a reduced locking time. And the buffer amplifier provides additional gain to compensate the smaller VCO output amplitude level. The phase noise at 1MHz offset is –120dBc/Hz, and the power consumption is 30mw.**

I. Introduction

The frequency of oscillators in RF transceivers must be defined with very high absolute accuracy. This often demands the use of phase-locked loops (PLL) in synthesizers because under the locked condition the output frequency of a PLL bears an exact relationship with the input frequency [1]. In addition to frequency accuracy, channel spacing, phase noise, sidebands and lock time are also the critical parameters of a synthesizer.

The lock time indicates how fast the new frequency is stabilized when the digital channel select input commands a change in the channel. A number of methods have been proposed to improve the channel switching behavior of the synthesizer. One type of methods is to add an extra startup circuit to suppress the normal operation of the circuits for a short period after the switching to help the system settling [2]. The other type of methods is to enhance the loop bandwidth, which can be determinative to the lock time [3].

In this paper, a fully integrated PLL-based frequency synthesizer for the 5GHz wireless LAN applications is presented using 0.25μm CMOS technology. The loop bandwidth enhancement is achieved simply by enlarging VCO tuning range. It gives extra bandwidth to get a reduced locking time. And the buffer amplifier provides additional gain to compensate the smaller VCO output amplitude level due to the enlarged tuning range. The phase noise at 1MHz offset is –120dBc/Hz, and the power consumption is 30mw.

II. Circuit Design And Operating Principle

The frequency synthesizer block diagram is shown in Fig. 1. The output frequency range is 5.17-5.33 GHz. It can be tuned to 8 channels, 23.5 MHz channel spacing. It uses an integer-N architecture. The output frequency is given by

$$f_{out} = f_0 + kf_{ch} \tag{1}$$

where f_0 is the frequency of the first channel (k=0), f_{ch} is the channel spacing. On the other hand, we have

$$f_{out} = 4f_{ref}(M_L + k) = 4M_L f_{ref} + 4kf_{ref} \tag{2}$$

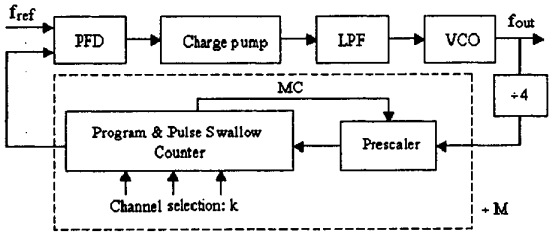

Fig. 1. PLL-Based Frequency Synthesizer Block Diagram.

Thus, $f_0 = 4M_L f_{ref}$ and $f_{ch} = 4f_{ref}$. Now we get f_{ref} =5.875 MHz, M_L=220. The frequency divider must provide a variable modulus given by M= M_L+k=220+k, k=0, 1, ..., 7. It consists of a +22/23 prescaler followed by a program and swallow counter.

A. Voltage-Controlled Oscillator (VCO)

Ring and LC oscillators are two widely used VCO types. Ring VCOs can generate quadrature signals more readily but have inferior noise performance, while LC VCOs offer better phase noise for a given power dissipation. In this design, we choose the LC VCO for the noise purpose.

The designed VCO is shown in Fig. 2. To get the negative resistance across the LC tank to guarantee the oscillation, we have taken the advantage of the impedance appearing at source terminal of a common-gate device. Practically, the cross-coupled differential pair is used to synthesize the negative resistance. The varactors used in this VCO are accumulation-mode MOS (A-MOS), achieved by connecting the drain and the source only, while add the control voltage on the bulk [4]. Since NMOS varactors are more sensitive to substrate-induced

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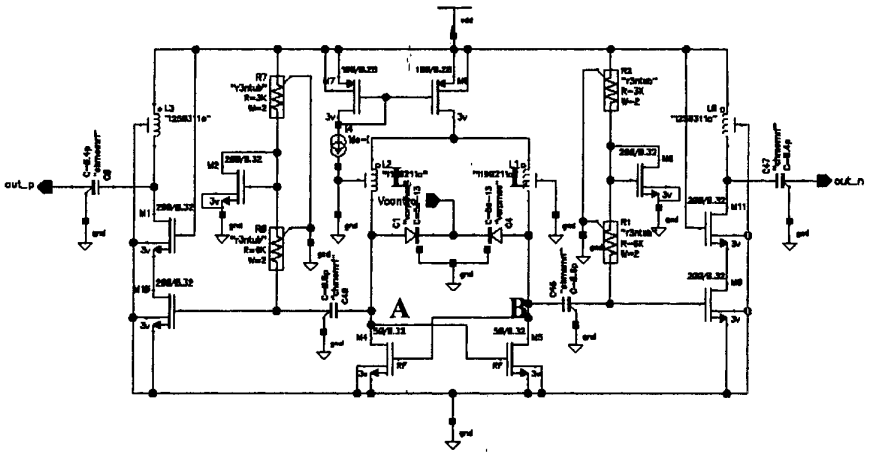

Fig.2. VCO with buffer amplifier.

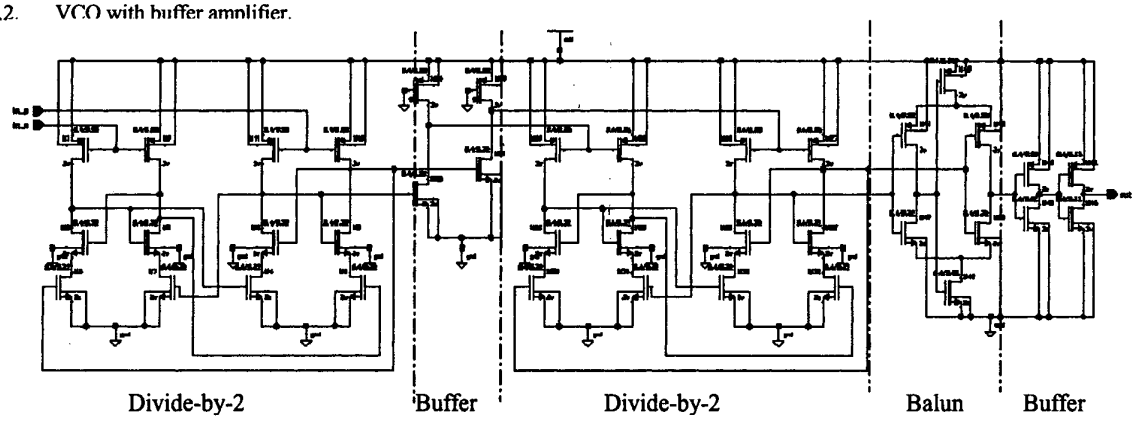

Fig. 3. Divide-by-4 circuit.

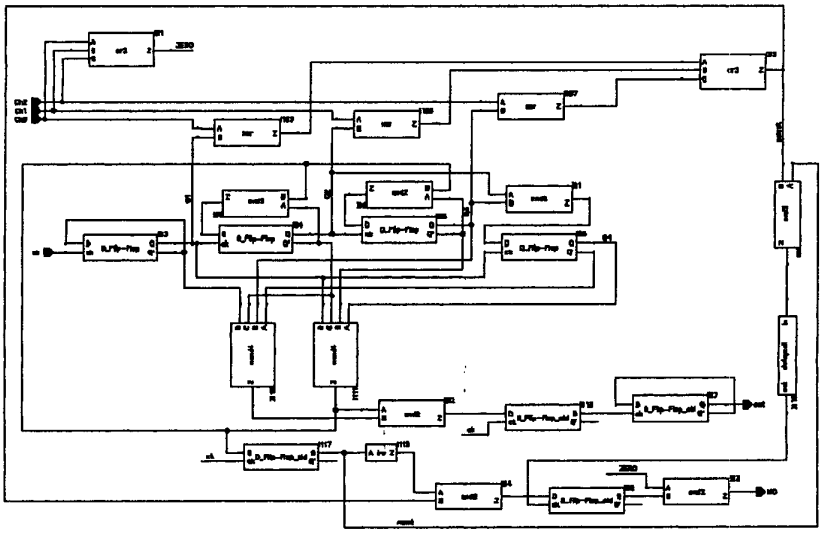

Fig. 4. Program and pulse swallow counter.

noise than PMOS varactors, we choose the PMOS device in our design.

The VCO core is symmetric, thus we can consider only half of the circuit. The resonance frequency is $\omega_r = 1/\sqrt{LC_{eq}}$, where C_{eq} is the equivalent capacitance seeing from point A or B. To achieve larger voltage swing, it is desirable to increase the value of the inductor L. However, for a given frequency, it means a smaller C_{eq}, which corresponds to a reduced output frequency tuning range. For resonance frequencies beyond 5GHz, the product of L and C_{eq} is rather small, making it difficult to get enough AC amplitude while maintaining an adequate frequency tuning range. To solve this problem, an amplifier stage is added after the oscillator.

B. Frequency Divider (÷4)

The prescaler (÷22/23) is a digital block. It cannot operate at an input above 2GHz. Therefore a high-speed divide-by-4 block is needed to lower the prescaler input frequency level. The proposed divide-by-4 circuit is shown in Fig. 3. Two high-speed frequency dividers [5] are put in series to get the divide-by-4 circuit. Between these two divider stages is a buffer circuit, which is made up of NMOS inverters. The reason not to use the CMOS inverter is that the output frequency of the first divider stage is still above 2.5GHz. The switching speed of PMOS transistor cannot meet this requirement. So PMOS is only connected as an active load.

The outputs of the second divider are differential, while the input of the next block (prescaler) is single-ended. A comparator acts as a balun in the circuit. Besides this, the output of comparator has sharper and smooth edges than the two input differential signals, further reduces the noise level of the system. An output buffer is after the balun to improve the driving capability.

C. Phase Frequency Detector (PFD), Charge pump & Loop Filter (LPF)

The phase frequency detector [1] can be used to detect both the phase and the frequency difference. If the frequency of input A, which is the reference, is leading, the output pulses will appear at QA; however, if B (feedback signal) is leading, output pulses will be at QB instead. QA and QB never have output at the same time.

The charge pump [6] consists of two switched current sources driving the second-order RC loop filter. For a pulse width T on QA, the current Ip deposits a charge IpT on the network. On the other case, if QB has the pulse, Ip will remove the charge, then driving the output voltage smaller. If no phase or frequency difference has been detected, QA=QB=0, and the output voltage remains constant.

The output of the loop filter is rising, giving a voltage from 0 to Vdd. An increasing VCO control voltage will make the VCO output frequency go higher, which can increase the feedback frequency.

D. Frequency Divider (÷M)

The divide-by-M block consists of a ÷22/23 prescaler followed by a program and swallow counter. The prescaler [7] consists of 4 divide-by-2/3 blocks and some other logic gates. The modulus control (MC) input selects between divide-by-22 and divide-by-23. The improved D-flip-flops used in the ÷2/3 circuits allow the prescaler to handle an input as high as about 2GHz.

The CMOS logic counter (shown in Fig. 4) generates one output pulse for every ten input pulses from the prescaler. The width of those input pulses is controlled by three channel select bits. At the beginning of each cycle, MC=1, the prescaler divides by 23. As soon as the lower three bits of the counter match the channel select bits, MC=0, the prescaler begins to divide by 22. The next cycle starts after the counter counts to ten. So the overall division ratio is 23*k+22*(10-k), which is 220-227, depending on the channel number k.

III. Simulation Results

Transient response of phase-locked loops is generally a nonlinear phenomenon that cannot be formulated easily. Nevertheless, as with other feedback systems, a linear approximation can be used to help PLL design. PLLs are best analyzed in the phase domain. It is instructive to calculate the phase transfer characteristic from the input to the output. The linearized mathematical model is shown in Fig. 5, where *Kvco*= 450MHz/Vfrom Fig. 6.

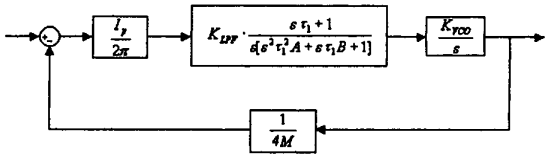

Fig. 5. Linearized PLL Model.

From the simulation, the PLL system achieves a phase margin of 50 degrees and the loop bandwidth about 600 KHz.

The phase noise is shown in Fig. 7, which is –120 dBc/Hz at 1MHz offset.

Fig. 8 shows the channel switching behavior of the system. At t=10μs, the channel changes from #4 to #0. The VCO control voltage achieves another stable value after about 3μs after switching.

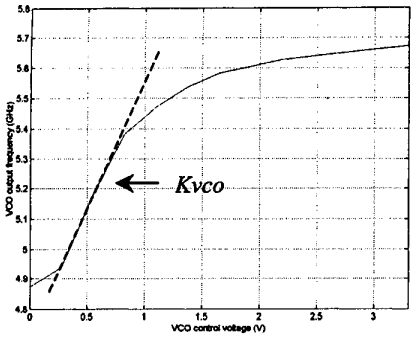

Fig. 6. VCO tuning range.

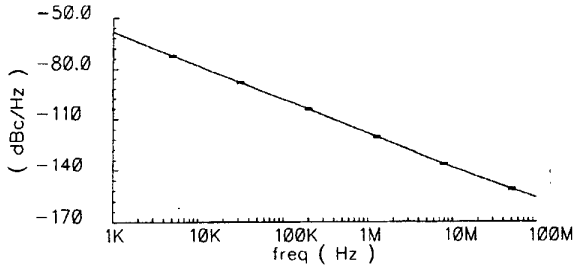

Fig. 7. Phase noise.

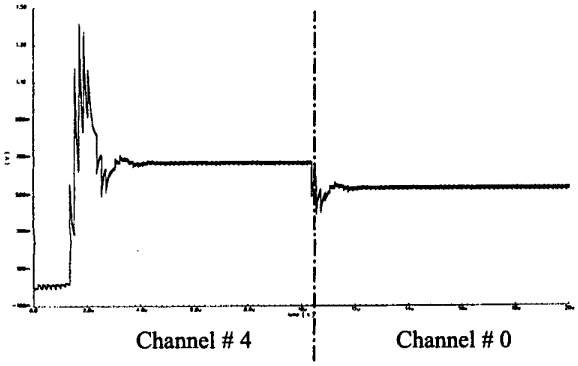

Fig. 8. VCO control voltage during channel switching.

IV. Conclusion

A fully integrated PLL-based frequency synthesizer for the 5GHz wireless LAN applications is presented using 0.25μm CMOS technology. The enlarging VCO tuning range gives extra loop bandwidth to reduce locking time when channel switching happens. The 3μs lock period shown in section III proves the validity of this fast switching method.

The relative smaller AC amplitude at the VCO output is compensated by the buffer amplifier, so that it won't affect the operation of the system. The phase noise at 1MHz offset is −120dBc/Hz, and the power consumption is 30mw. The performance of the proposed synthesizer is summarized in TABLE I.

TABLE I
SUMMARY OF THE PERFORMANCE

Frequency Range	5.17 GHz – 5.33 GHz
Channel Spacing	23.5 MHz
VCO Tuning Range	800 MHz
Power Supply	3.3 V
Total Power	30 mw
VCO power	15 mw
Lock Time	3 μs
Phase Noise	-120dBc/Hz at 1MHz offset

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